CYCLOS SEMICONDUCTOR ANNOUNCES INDUSTRY BREAKTHROUGH FOR LOW POWER DESIGN USING CADENCE LOW POWER SOLUTION

*Cadence Encounter Platform is selected for industry’s first high-performance power-efficient resonant clocking design methodology*

San Jose, CA, and Berkeley, CA – June 9, 2008 – Cyclos Semiconductor, Inc., a privately-help start-up company and pioneer of resonant-clock design technologies for ultra-low-power devices, today announced the Cyclify back-end design flow for resonant-clock ASIC design. The breakthrough Cyclify flow uses the Cadence Low Power Solution to enable design of low-power applications in the embedded, mobile, medical, and compute server space with extreme low-power and low-electromagnetic-interference requirements. Used in conjunction with the Cyclos Resonant-Clock (RCL) Platform, Cyclify is the industry’s first back-end design flow for seamlessly integrating resonant-clocking into ASIC designs, addressing the needs of designers for fast turnaround times, robust design, and high-performance low-power implementations.

By achieving unprecedented levels of clock power savings, resonant clocking enables designers to include additional functionality within their power budget, enabling designers to achieve high performance targets with unprecedented levels of power efficiency. Within a commercially available industry-standard design environment, Cyclify provides all the benefits of clocked design without the power consumption, peak currents, and supply/ground bounce issues typically associated with clocking. In addition to power savings, Cyclify can lead to higher-performance designs and shorter design cycles by reducing the performance penalties and verification overheads typically associated with other clock power reduction approaches such as clock gating. Moreover, by reducing the number of active devices required for clock distribution, it can also provide increased tolerance to PVT variations.

Cyclify is compatible with existing power reduction approaches such as clock gating, power gating, multiple thresholds, and multiple voltage domains, providing additional power benefits. Moreover, it is compatible with system-on-chip (SOC) design
approaches. Operating at the back-end of the design flow, Cyclify is architecture-agnostic and can be applied transparently to any synthesized design with no changes to synthesized netlists or verification vectors. Designers can easily use the new flow with any standard cell library and any front-end EDA tools.

“As we continue to extend our leadership in providing advanced low-power design solutions, it is exciting to work with innovative companies to advance the state-of-the-art in power reduction technologies,” said David Desharnais, group director of IC Digital products at Cadence. “Using the Encounter Platform as part of our overall Cadence Low Power Solution, Cyclos has achieved the industry’s first ASIC design methodology integrating resonant clocking, thereby extending battery life in embedded and mobile applications and reducing power requirements in high-performance applications.”

“We are pleased to announce this breakthrough in power reduction technology and make it accessible to the broader ASIC design community,” said Alexander Ishii, VP of Engineering, Cyclos Semiconductor. “This is a milestone for our company, and we appreciate Cadence’s low power expertise and contributions to this development. A primary goal has been to deploy the technology with a minimum of disruption to a traditional ASIC/SOC development flow and design platform. We were able to produce working first-silicon pilot chips using standard out-of-the-box Cadence tools.”

Customers can design their own low-power resonant-clock designs by licensing the Cyclos Cyclify flow and RCL Platform directly from Cyclos. Alternatively, Cyclos offers design services for integrating the Cyclos RCL Platform into customer designs. More information on Cyclos Semiconductor, Inc. and its products can be found at http://www.cyclos-semi.com.
About Cyclos

Cyclos is a privately-held start-up company commercializing next-generation ultra-low-power design technologies. Silicon-proven on high-end ASIC designs, Cyclos technology provides unprecedented power efficiency at max-performance clock speeds. It is available to customers via general-purpose libraries, ultra-low-power IP cores, and customer-specific-design services. Compatible with standard design flows, Cyclos technology allows customers to deliver class-leading devices to power-critical markets such as mobile, wireless, medical, and general-purpose computing. More information about the company is available at www.cyclos-semi.com.

About Cadence

Cadence enables global electronic-design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence® software and hardware, methodologies, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. Cadence reported 2007 revenues of approximately $1.6 billion, and has approximately 5,100 employees. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at www.cadence.com.

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