CYCLOS SEMICONDUCTOR, INC., ANNOUNCES AVAILABILITY OF INDUSTRY'S FIRST PLATFORM-IP FOR RESONANT-CLOCK ASIC DESIGN

New Resonant Clock Platform offers IP cell libraries for low-power resonant-clock chips.

Berkeley, CA – June 9, 2008 – Cyclos Semiconductor, Inc., a privately-held start-up company and pioneer of resonant-clock design technologies for ultra-low-power devices, today announced the availability of the Resonant Clock (RCL) Platform for low-power ASIC design. Targeting applications in the embedded, mobile, medical, and compute server space with extreme low-power and low-electromagnetic-interference requirements, RCL is the industry’s first platform IP for standard-cell-based design and seamless interfacing of resonant-clocked chips. Currently, RCL has been silicon-verified in conjunction with the Cyclify standard-cell design flow on the standard-threshold UMC 130nm bulk silicon process.

By enabling the automatic integration of resonant clocking, RCL yields chip designs with significantly reduced clock power, enabling designers to include additional functionality within their power budget or, alternatively, high performance targets with unprecedented levels of power efficiency. Compatible with commercial EDA tools, the Cyclos RCL Platform provides all the benefits of clocked design without the power consumption, peak currents, and supply/ground bounce issues typically associated with clocking. In addition to power savings, RCL can lead to higher-performance designs and shorter design cycles by reducing the performance penalties and verification overheads typically associated with other clock power reduction approaches such as clock gating. Furthermore, by reducing the number of active devices required for clock distribution, it can lead to designs with increased tolerance to PVT variations.

The Cyclos RCL Platform includes flip-flops and clock generators for resonant-clock chip design. It also includes cells that enable the interfacing of resonant and conventional clock domains. RCL is compatible with other standard-cell libraries developed for the same process, such as the ARM Metro and the Synopsys DesignWare libraries. It is also compatible with existing power reduction design methodologies such as clock gating, power gating, multiple thresholds, and multiple voltage domains, providing additional
power benefits. Furthermore, it is compatible with system-on-chip (SOC) design methodologies. The Cyclos RCL Platform is architecture-agnostic and can be used to implement any synchronous (clocked) design without changing synthesized netlists or verification vectors.

“UMC is pleased that Cyclos has chosen our L130E process for its first RCL low-power IP technology offerings. This selection demonstrates UMC's position as a leading low-power silicon foundry and provides current and future UMC customers with a new source for clocking technology,” said KC Wang, Chief Engineer of System & Architecture Support at UMC. “We look forward to expanding our partnership with Cyclos to include additional low-power offerings for our performance-oriented customers.”

“The Cyclos RCL Platform has been designed to fully support the automated design of resonant-clock chips with design efficiencies and design cycles surpassing those of ASIC design methodologies,” said Alexander Ishii, VP of Engineering, Cyclos Semiconductor. “By selecting UMC’s 130nm bulk silicon standard process as its first RCL Platform offering, Cyclos makes its innovative power-reduction technology accessible to a very broad community of designers that are sensitive to low power requirements.”

Customers can design their own low-power resonant-clock designs by licensing the Cyclos RCL Platform and Cyclify flow directly from Cyclos. Alternatively, Cyclos offers design services for integrating the Cyclos RCL Platform into customer designs.

About Cyclos
Cyclos is a privately-held start-up company commercializing next-generation ultra-low-power design technologies. Silicon-proven on high-end ASIC designs, Cyclos technology provides unprecedented power efficiency at max-performance clock speeds. It is available to customers via general-purpose libraries, ultra-low-power IP cores, and customer-specific-design services. Compatible with standard design flows, Cyclos technology allows customers to deliver class-leading devices to power-critical markets.
such as mobile, wireless, medical, and general-purpose computing. More information about the company is available at www.cyclos-semi.com.

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